

Autonomous Driving: And the Impact of People, Process & Technology

WIND

Marques McCammon

Automotive Solutions

July 16, 2015

Roadmap to Autonomy



For more than 30 years, when industry sets out to build something that **must work**, they've turned to Wind River



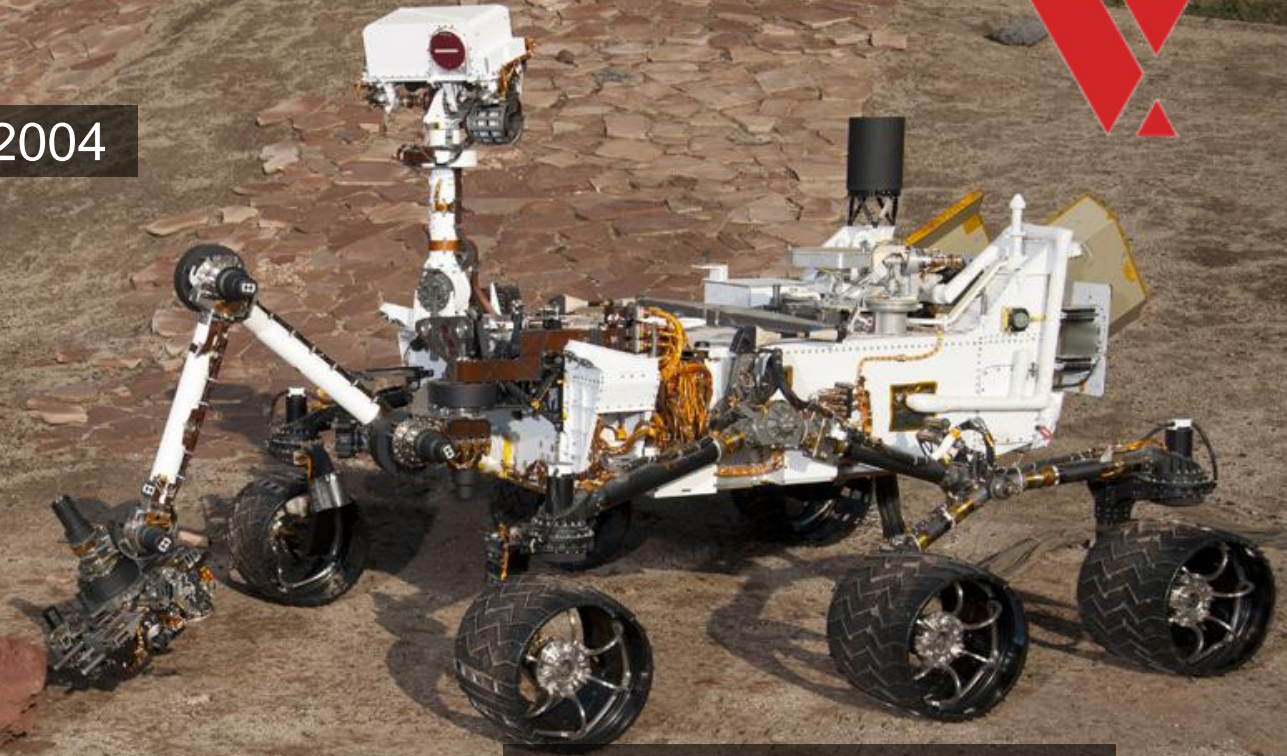
Pedigree



Spirit/Opportunity, 2004



Sojourner, 1997



Curiosity, 2012

Wind River has been a part of every Mars Lander since 1997



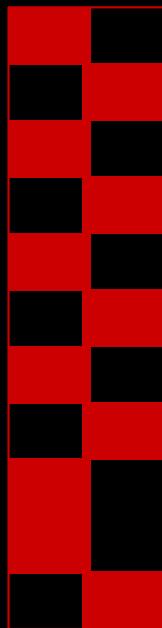
caps lock

change





JPL



Mars Teams

NASA / JPL

+ Academia

+ Industry (component)

+ Silicon Valley

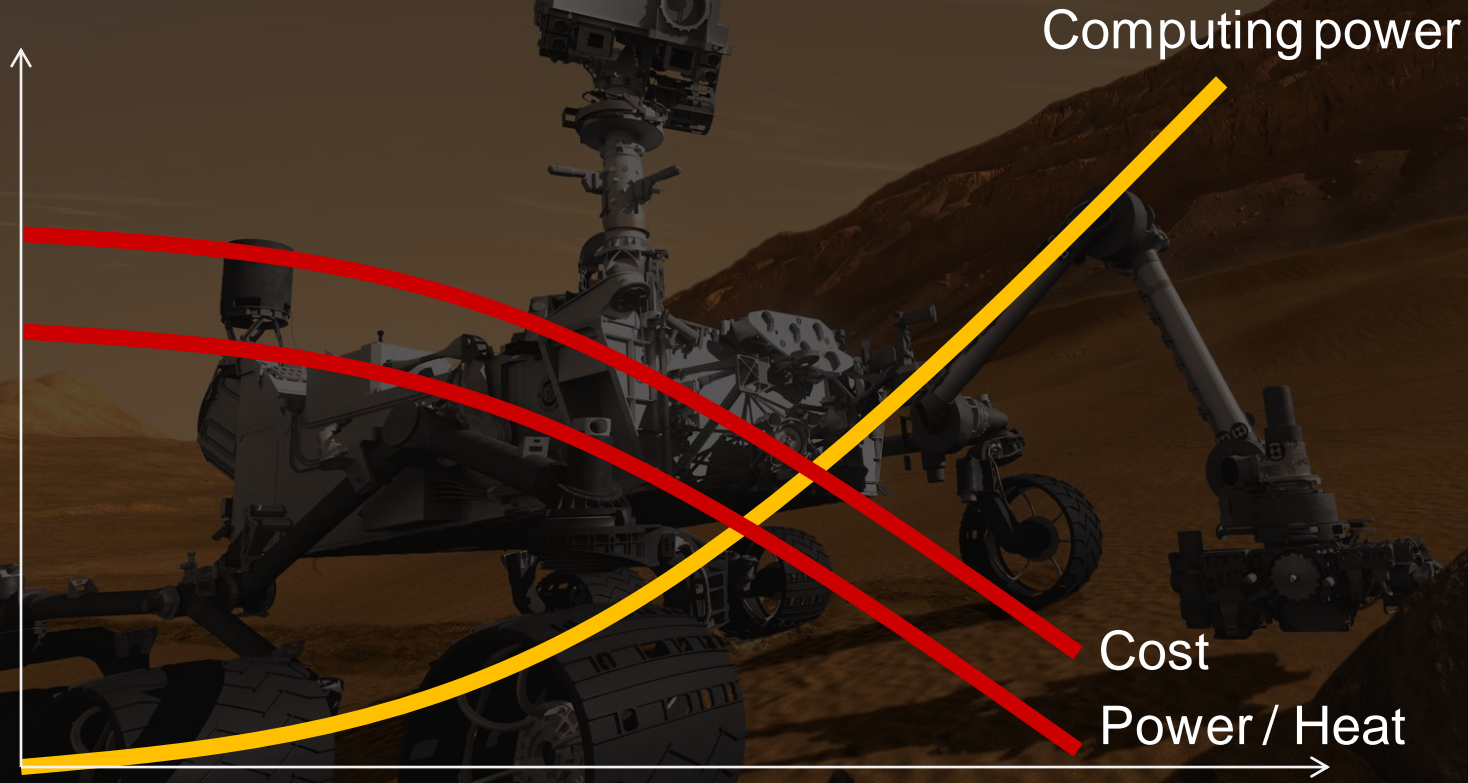
Disaggregate supply chain

Shift to systems integration

Inter-corporate Design and Release



Technology - Moore's Law



Cyber Security

High Performance
Computing

Vehicle Safety
& Regulation

Consumer Electronics

Automotive
Industry

Digital Consumerism

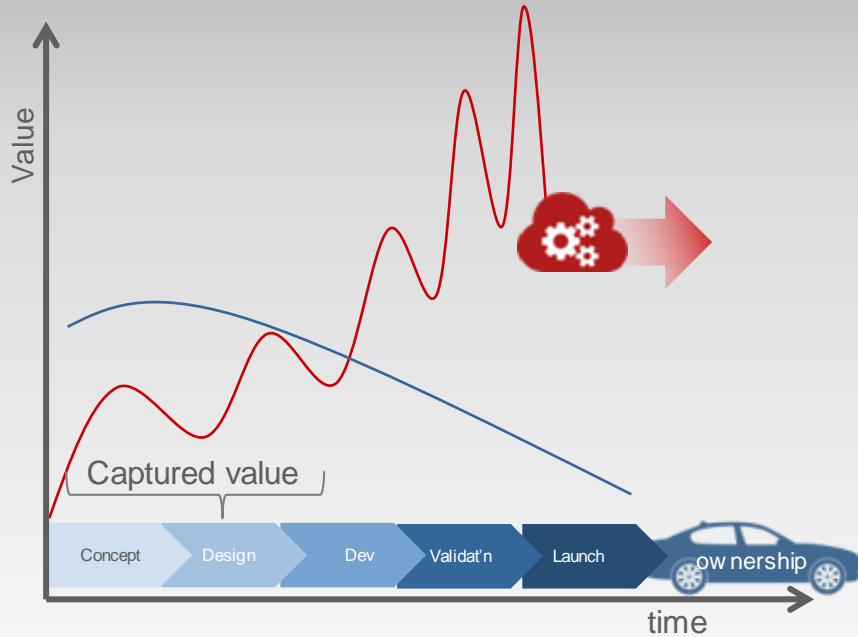


Key Questions?

- What is the model for software in the future of Automotive?
- How is the ownership divided?
- Where does the value live?
- Can Automotive move at the pace of innovation?
- How will the fundamental business of Automotive change?
- How do you protect the consumer and enable the consumer at the same time?
- Who accepts the risks?
- How do you make money?

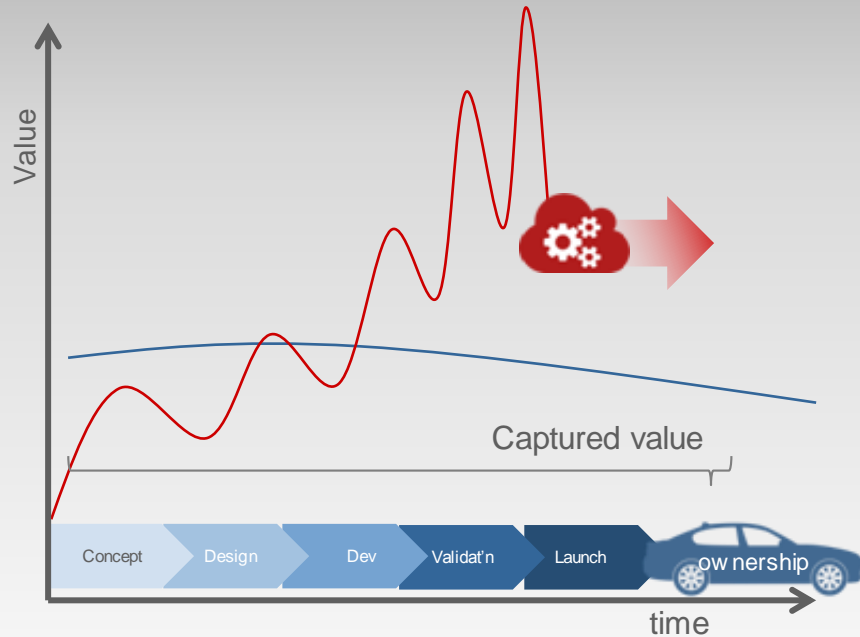


The Goal: Automotive Software Integration at the Speed of Innovation



Automotive development cycles are grossly out paced by the speed of software innovation leaving cars obsolete even before they are shipped

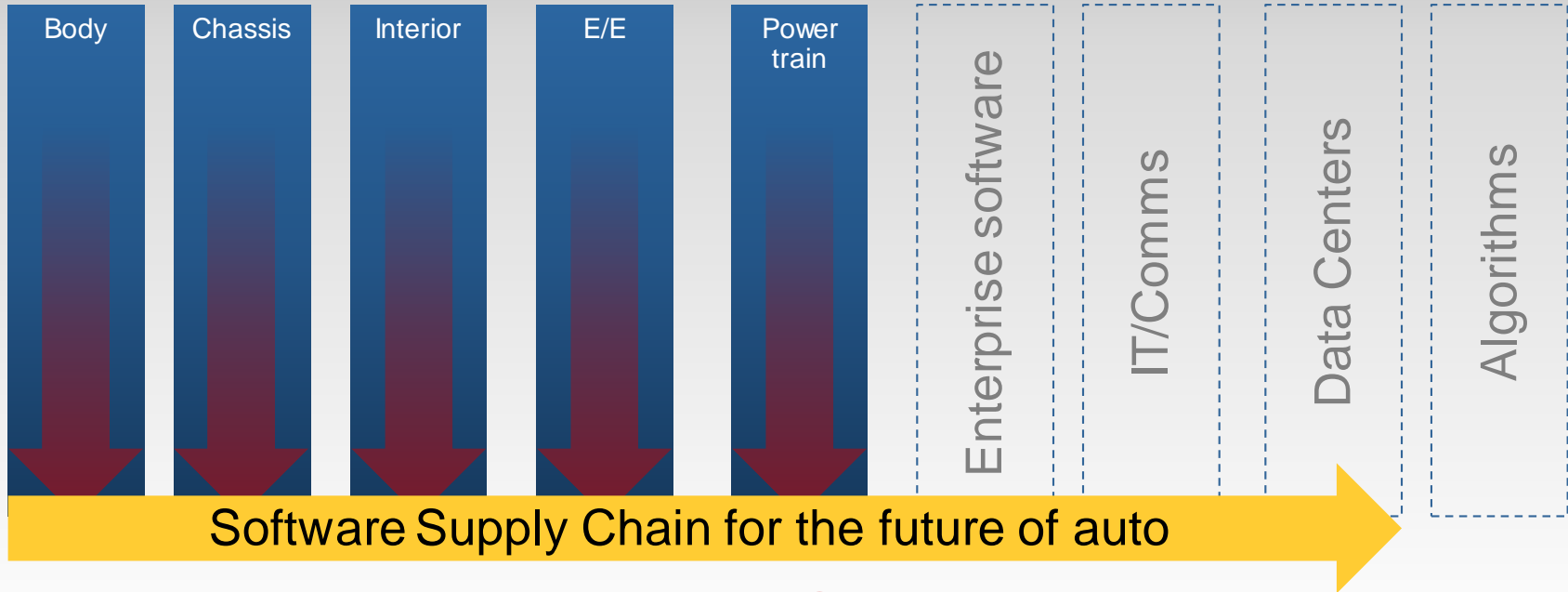
The Goal: Automotive Software Integration at the Speed of Innovation



Automotive needs a mechanism to capture the increasing software value across the vehicle lifecycle without creating risk to the function of the underlying architecture

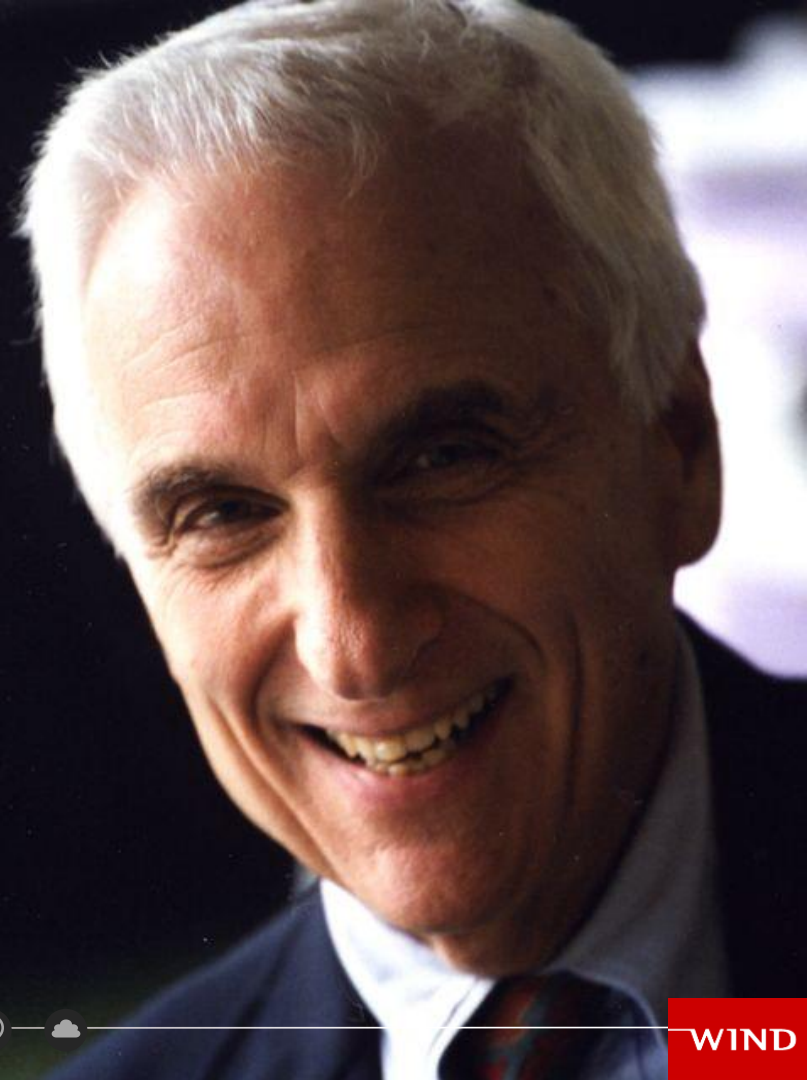
New Supply Models

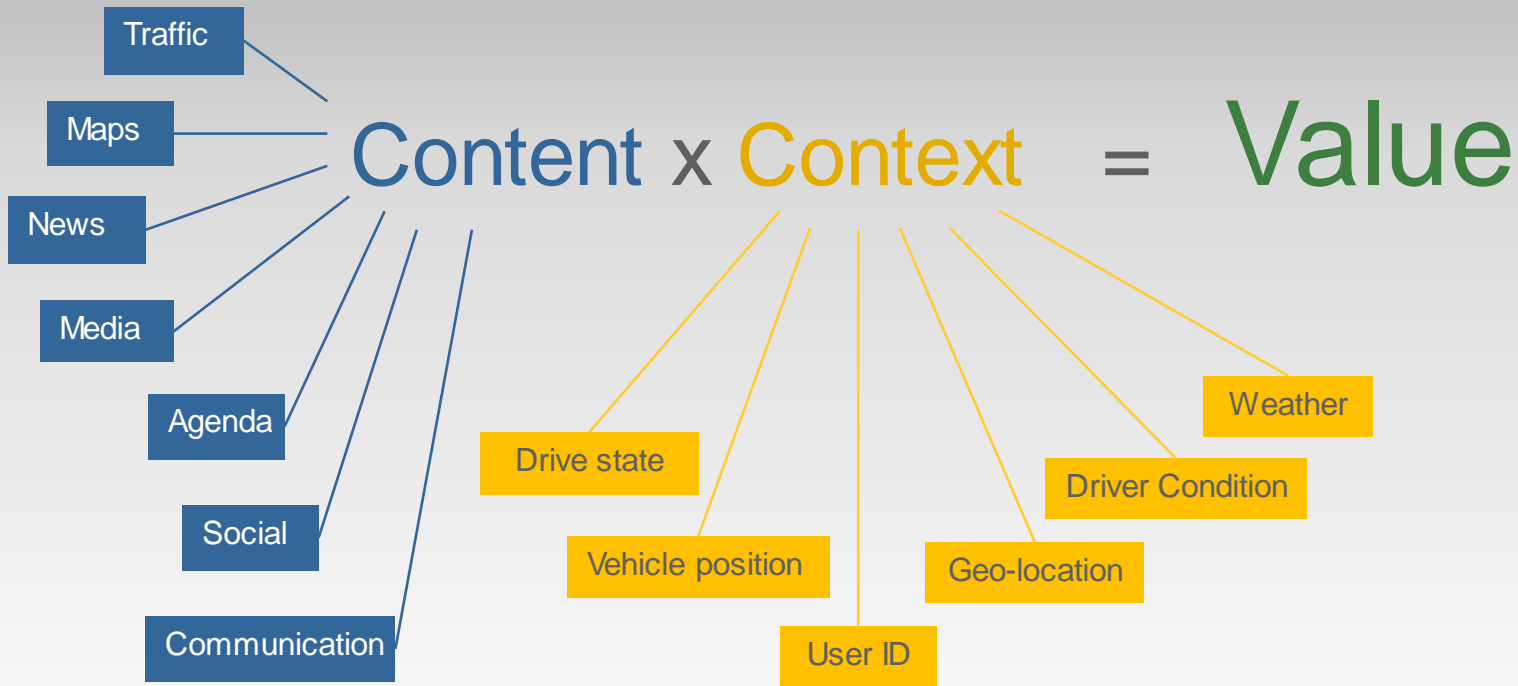
Conventional Supply Chain Alignment



“ ...organizations which design systems ... are constrained to produce designs which are copies of the communication structures of these organizations ”

Melvin Conway







Bottom line:

1. Cost
2. Speed
3. Extensibility
4. Risk Management
5. Innovation



The Era of Autonomous Driving...

and its Implications for Electronics System Designers

Wind River Webinar, July 15, 2015

Michael Hendricks, Automotive & Consumer PLM

Clive Davies, Automotive System Architect



Automotive Electronics

- ◀ Electronic proliferation in vehicles creating a boom market for automotive semiconductors
 - In **2005** electronics comprised **15 percent** total cost of vehicle*
 - In **modern hybrid vehicles** electronics represent **45 percent** of cost*
 - ◀ Up to 50 percent of standard vehicles in near future
 - ◀ Up to 80 percent of hybrids in near future
- ◀ Processing requirements skyrocket
 - Up to 100 electronic control units (ECUs) in today's vehicles
 - ◀ Trend toward sensor fusion and ADAS centralized architectures
 - Processor performance in vehicles to **increase 100x by 2024**
- ◀ Software complexity
 - Modern premium automobiles now have ~100 million lines of code

Sources: [IEEE Spectrum – This Car Runs on Code](#)
ARM Holdings

What is Driving Electronics Growth in Automotive?

Consumer Demand

- Audi's electronics enabled features responsible for \$9,600 increase in average transaction prices for Audi U.S. over last five years
 - **"Our cars are the grandest and most beautiful electronic devices on the planet,"** Prof. Dr. Ulrich Hackenberg, Audi Board Member Tech Development



Audi Digital Instrument Cluster

Safety

- 1.2 million road fatalities each year
- 90% caused by human error

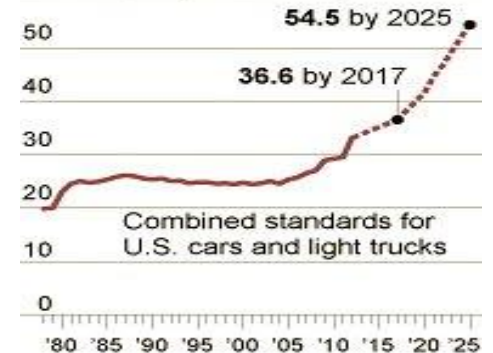


Efficiency / Environment

- "A hybrid electric vehicle demands **ten times more semiconductor content** in powertrain"
 - Ahad Buksh, IHS analyst, automotive semiconductors

New Goals in Fuel Economy

60 miles per gallon average fleetwide



Source: National Highway Traffic Safety Administration

Automotive Mega Trends & Key Requirements

Cockpit Evolution Cluster, HUD, HMI, CID



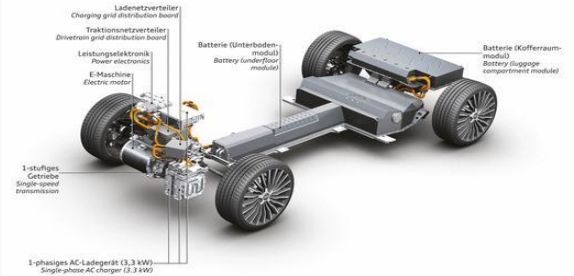
- **Why FPGA:**
 - Special feature / function
 - IO expansion
 - Video connectivity

Self-Driving Car Camera, Radar, Laser



- **Why FPGA:**
 - Evolving algorithms
 - Performance / Watt
 - Differentiation vs. ASSP
 - Scalability

EV / Powertrain BMS, Motor Control, ECU



- **Why FPGA:**
 - Real-time parallel processing
 - Faster control loops
 - Enables better motors



Functional Safety

Video & Vision Processing

SW Development Flows

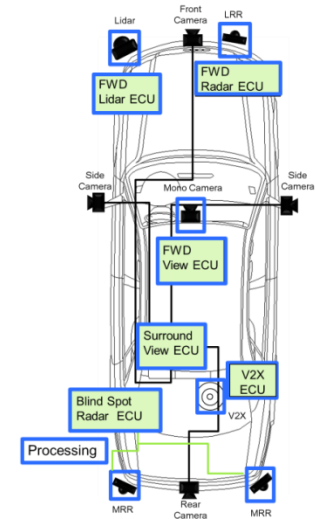
Infotainment & Driver Information

ADAS

EV & Powertrain

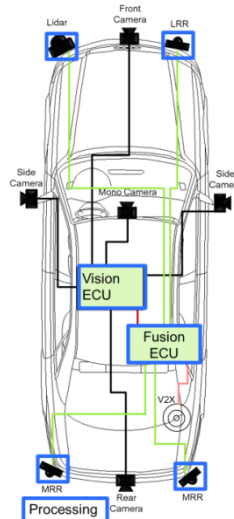
ADAS Architecture Trends – Scalable Platform Required

Distributed



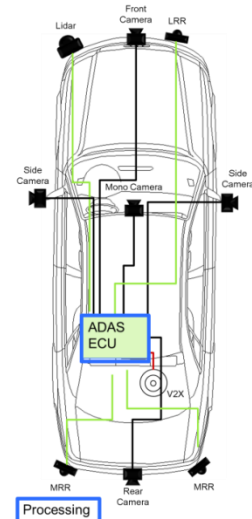
~3K DMIPS/ECU

Partially Centralized

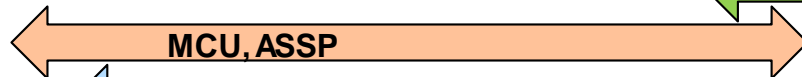


~10K DMIPS/ECU

Centralized



~15K+ DMIPS/ECU



MCU, ASSP



ASSP, GPU, CPU



ALTERA

Scalable FPGA Platform
(Spans all architectures)

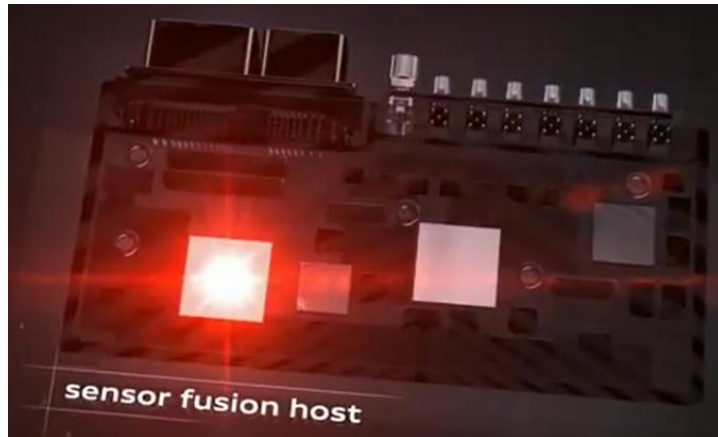
ALTERA

Audi & TTTech Select Cyclone V SoC for Audi zFAS Piloted Driving ADAS

Altera's SoC FPGAs integrate a **flexible fabric and CPU** that enable us to deliver leading-edge **communication safety and a vastly accelerated, yet very robust software integration** process to Audi on their way towards the vision of piloted driving. **FPGAs are well-suited to manage this type of complex computing and networking.** They still remain an **affordable and low-power solution.**

—Dr. Stefan Poledna, TTTech co-founder and board member

Audi zFAS Block Diagram



Sources: [Green Car Congress](#), Altera, TTTech
Video: [Audi - Piloted Driving. zFAS - All functions. one unit](#)



Why Altera

- ISO 26262 Support
 - ◀ Functional Safety Data Pack
 - ◀ ECC on memory
- Integrated transceivers
 - ◀ Communication to GPU
- Highest logic density
Automotive SoC-FPGA



Audi zFAS PCB



Functional Safety – Priority

- Functional safety is to prevent the risk of **injury or death** as a result of **random, systematic, or common-cause failures** in safety-relevant systems

Functional Safety
Data Package (FSDP)

Save
≈18-24
months!
TTM



Methodology

Tools

IP

PLDs

SUPPORT RESOURCES

QUALITY

- ISO/TS 16949
- AEC Q100
- ISO 9001

DOCUMENTATION

- Functional Safety Data Package (FSDP)
- APP Notes, REL Reports

CERTIFICATION

- Devices
- IP (Dia., μ C, IP)
- Design Flow
- Tools

STANDARDS

- IEC61508 Industrial
- ISO26262 Auto

Technological Changes



The Need For Change

~~Moving to a smaller process node gets you~~

- ~~– More performance~~
- ~~– Better power efficiency~~
- ~~– Lower cost~~

These assumptions are no longer valid!

- Getting harder and harder to scale down process geometry
- Costs are rising

We need to find other ways to improve system performance

- New ways of thinking
- Not just “like the last version, but faster”

Huge increase in processing while maintaining power envelope

- Microsoft whitepaper shows FPGA significantly more power efficient than GPU for Convolutional Neural Networks (CNNs)

New Ways of Thinking

◀ Changes for system developers

- Move to heterogeneous solutions
- Re-think system partitioning
- Adopt new platform technologies

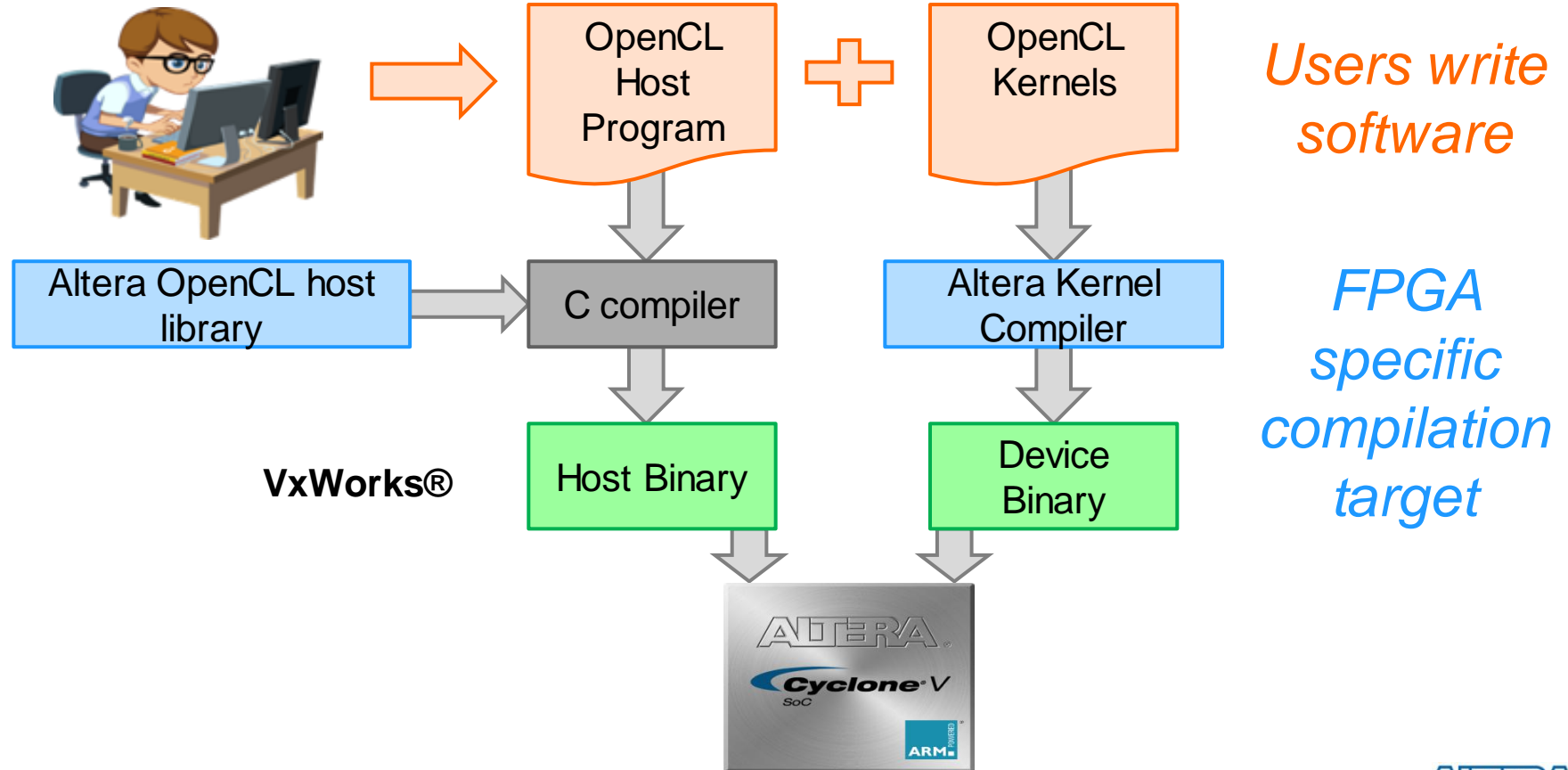
◀ Changes for technology suppliers

- Think about system programmability
- Address new classes of developers
- Develop system programming tools

◀ Example: Altera's OpenCL compiler

- Bringing FPGA performance to software engineers

Programming FPGAs : SDK for OpenCL



OpenCL Design Approach for Dense Optical Flow

Step 1: Whitepaper to C implementation

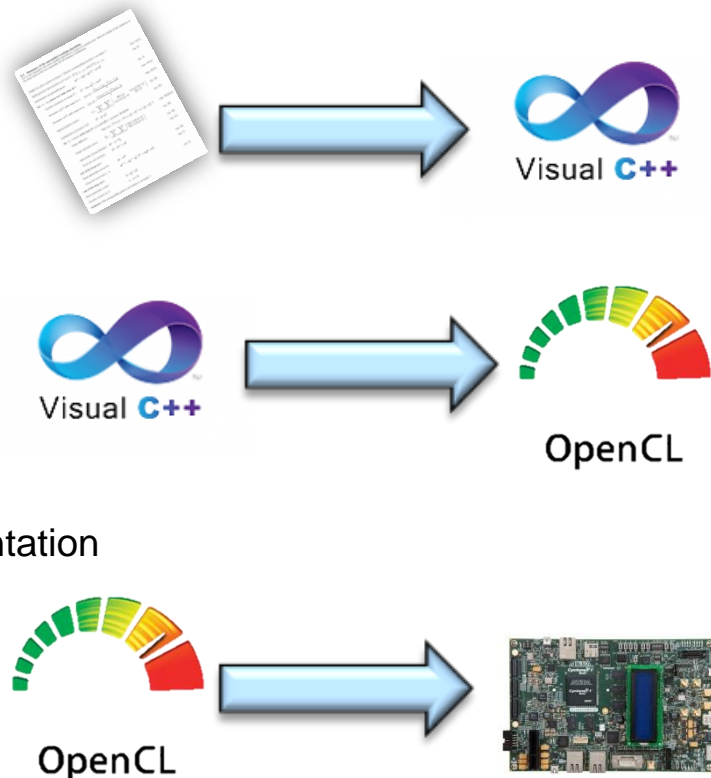
- Pyramidal Lucas Kanade optical flow
- Easy to check implementation
- Prove C implementation

Step 2: C implementation to OpenCL

- Optimisation stage
- Port linear C implementation to parallel OpenCL implementation
- C model allows checking of OpenCL output

Step 3: OpenCL to hardware

- Final stage to target OpenCL to hardware
- Dealing with board/video startup



Example Design

Lucas Kanade Optical Flow Developed with OpenCL

Applications:

- Pedestrian, vehicle, object tracking and recognition
- Collision avoidance, blind spot detection, AEB

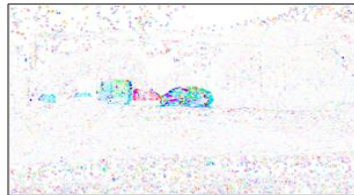


Algorithm Performance:

- Dense flow
- 720p Image resolution, 60 fps
- 2 frames latency...

OpenCL Design Methodology

- No RTL coding required
- Original algorithm in C
- 3 weeks to convert to OpenCL and target FPGA



FPGA Implementation:

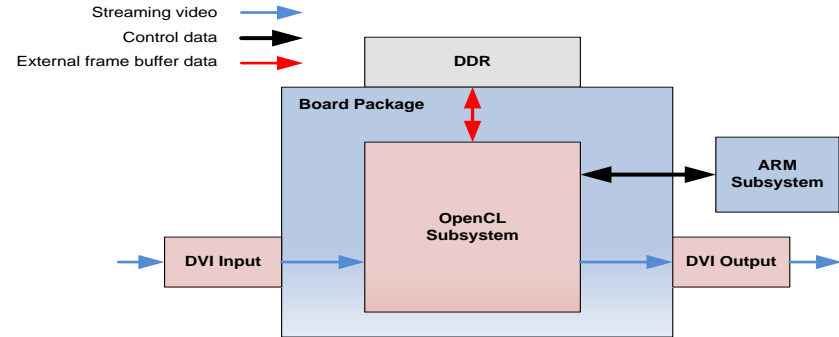
- Cyclone V SoC
- 55K LE, 50% of device
- 68% memory, 44% DSP utilization ...



ALTERA

© 2014 Altera Corporation. All rights reserved. ALTERA, ARRIA, CYCLONE, ENPERION, MAX 10, MEGAACORE, NIOS, QUARTUS and STRATIX words and logos are trademarks of Altera Corporation and registered in the U.S. Patent and Trademark Office and are trademarks or registered trademarks in other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders as listed at www.altera.com/legal.

For info: Automotive@altera.com



DVI output



DVI input



Optical Flow Design Example

ALTERA

Summary

- ◀ Rapid increase in electronic content of vehicles
- ◀ Processing requirements increasing rapidly
 - Existing architectural approaches can't keep pace
- ◀ Design cycles getting shorter and shorter
- ◀ Need new ways of thinking to address these issues

Additional resources:

Altera's OpenCL SDK: <https://www.altera.com/products/design-software/embedded-software-developers/opencl/overview.html>

OpenCL Optical flow example: <https://www.altera.com/support/support-resources/design-examples/design-software/opencl/optical-flow.html>

Microsoft whitepaper on CNNs in FPGA:
<http://research.microsoft.com/pubs/240715/CNN%20Whitepaper.pdf>

Q & A

